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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,472	08/29/2001	Katsuji Kimura	Q65962	4891

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SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.
Washington, DC 20037

EXAMINER

NGUYEN, MINH T

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,472	KIMURA, KATSUJI	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3 and 4 is/are rejected.
- 7) ☒ Claim(s) 2 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's amendment filed on 2/6/04 has been received and entered in the case. Claims 1-4 are pending. The amendment and argument presented therein overcome the informality objections, and therefore, are withdrawn. New ground of rejection necessitated by the amendment is set forth below. This action is FINAL.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 3, the recitation on the last line is unclear and confusing, i.e., it is unclear if the recited "current source" on the last line and the recited "constant current source" on line 8 are the same current source. If they are the same, the same name should be used. If they are different, please clarify. In the remarks section filed on 2/6/04, page 4, the applicant vaguely indicates that the recited current source is shown in Figs. 1-3 and 6-17, however, it is unclear where it is in the Figs. Further, it is unclear where the recited "constant current source" is in addition to the recited "current source".

As per claim 4, the claim is rejected because of the indefiniteness of claim 3.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,602,509, issued to Kimura.

Kimura discloses a voltage adder/adder circuit (Fig. 3) comprising:

a differential pair (1) having a first MOS transistor M1 and a second MOS transistor M2, wherein the gate electrodes of the first and second MOS transistors forming input terminals, i.e., the gate terminals of M1 and M2, for receiving an input differential voltage (V_i), the drain electrodes forming output terminals to the subtractor circuit (3) for outputting signals ($ID1$ and $ID2$) to be subtracted by the subtractor (3), and source electrodes of M1 and M2 commonly coupled to form an output terminal (the common source node) for outputting a voltage to be added (the voltage at the common source node); and

a constant current source (the source which provides the current I shown in box 2, also see column 2, line 21) which drives the differential pair (1); and

a current source (the current corresponding to the second term of the formula shown in box 2, i.e., the term $(\beta/2)*V_i^2$) coupled between ground and the commonly coupled source electrodes.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No.

5,602,509, issued to Kimura.

Kimura discloses a voltage subtract or/adder circuit (Fig. 3) comprising:

a current subtractor (3) for providing an output terminal for outputting an output current ΔI in proportion to the subtraction of two input voltages (one is at the gate of M1 and the other one is at the gate of M2);

a differential pair (1) having a first MOS transistor M1 and a second MOS transistor M2, wherein the gate electrodes of the first and second MOS transistors forming input terminals for receiving the input voltages (the input voltages at the gates of M1 and M2), the drain electrodes of the first and second MOS transistors supplying a differential current to the current subtractor (the I_{D1} and I_{D2} currents) to the subtractor (3), and source electrodes of M1 and M2 coupled to form an output terminal for outputting an addition output voltage in proportion to half of the addition of the two input voltages (see the formula in box 2);

wherein the sum of currents flowing through the M1 and M2 increases in proportion to the square of a difference of the two input voltages (see the formula shown in box 2, the V_i^2 term is clearly met this recited function); and

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a current source (the current corresponding to the second term of the formula shown in box 2, i.e., the term $(\beta/2)*V_i^2$) coupled between ground and the commonly coupled source electrodes.

Kimura does not explicitly disclose a current to voltage converting means for providing an output voltage in proportion to the subtraction of two input voltages as called for in the claim.

The Examiner takes Official Notice the fact that using a resistor to convert a current into voltage is old and well known in the art, i.e., using Ohm's Law, $V=RI$, and the practice is well-known in the electronic field.

It would have been obvious to one skilled in the art at the time of the invention was made to connect a resistor to the output of the subtractor circuit (3) in the Kimura circuit shown in Fig. 3 to convert the $\Delta(I)$ current into voltage.

The motivation and/or suggestion for doing so would have been to allow the Kimura circuit to be able to interface with another circuit which requires the input signal is a voltage signal instead of current signal.

Response to Arguments

5. Applicant's arguments filed on 2/6/04 have been fully considered but they are not persuasive.

Regarding the argument the reference does not disclose a current source (newly added limitation). Please see the preceding rejection for the identification of the recited current source.

Regarding the argument the reference fails to teach an output terminal for outputting a voltage to be added.

The “commonly connected source electrodes” node of the differential pair reads on the output terminal. The examiner notes that the claim language does not require the output terminal node being distinct from the “commonly connected source electrodes” node of the differential pair, i.e., it only requires the “node” being capable of providing a signal which is proportion to half of the additional of two input voltages. The examiner further notes that even the claim requires an output terminal connected to the “commonly connected source electrodes” node of the differential pair as argued by the applicant, such requirement is seen as an obvious modification and is well within the level of one skilled in the art.

Regarding the argument it is not obvious to convert a current signal to a voltage signal, i.e., converting the addition current (ΔI) to a voltage at the output.

The examiner notes that Ohm’s Law, which is notoriously well-known ($V=RI$), clearly teaches this feature. The teaching can be found in many electronic textbooks.

Allowable Subject Matter

6. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 2 is allowable because the prior art of record fails to disclose or suggest the inclusion of a level shifter for level shifting the addition output voltage. The prior art of record taught a level shifter for level shifting the addition *current level* not the addition output voltage as required in the claim and it appears that there is no motivation and/or suggestion either in the

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reference or using commonly knowledge by a person skilled in the art at the time of the invention was made to modify the prior art circuit to obtain the circuit recited in the claim.

7. Claim 4 would be allowable for the same reason noted in claim 2, if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



4/9/04

Minh Nguyen
Primary Examiner
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